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EXAMINER	
LANDAU, MATTHEW C	
ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 04/27/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/726,911	MIN ET AL.	
	Examiner	Art Unit	
	Matthew Landau	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 April 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-34* is/are pending in the application.

4a) Of the above claim(s) *17-34* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

Applicant's election with traverse of Group I, claims 1-16, in the reply filed on April 8, 2005 is acknowledged. The traversal is on the ground(s) that simultaneous examination of all claims would not present an undue burden since the two inventions are "classified commonly in class 438". This is not found persuasive because the device claims of Group I are in fact classified in a different class (class 257) than the method claims of Group II, which are classified in class 438.

The requirement is still deemed proper and is therefore made FINAL.

Claims 17-34 are withdrawn from further consideration pursuant to 37 CFR 1.142(b), as being drawn to a nonelected invention, there being no allowable generic or linking claim.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-3, 6, 8-10, 12, and 13 are rejected under 35 U.S.C. 102(b) as being anticipated by Shimoji (US Pat. 5,349,222).

Regarding claims 1-3, Figure 3 of Shimoji discloses a control gate pattern disposed over a semiconductor substrate 2 and comprising a tunnel insulation pattern, a trap insulation pattern, a blocking insulation pattern, and a control (memory) gate electrode 5, which are stacked; a selection gate electrode 23 disposed over the semiconductor substrate at one side of the control gate pattern; a gate insulation pattern 8 interposed between the selection gate electrode and the semiconductor substrate, and between the selection gate electrode and the control gate pattern; a cell channel region comprising a first channel region defined in the semiconductor substrate under the control gate pattern and a second channel region defined in the substrate under the selection gate electrode. Note that region 6 under the control gate is an ONO layer (silicon oxide/silicon nitride/silicon oxide) (col. 5, lines 28-32). The first silicon oxide layer 6a is the tunnel insulating pattern, the silicon nitride layer 6b is the trap insulation pattern, and the second silicon oxide layer 6c is the blocking insulation pattern.

Regarding claim 6, Figure 3 of Shimoji discloses a drain region 3 in contact with the first channel region and a source region 4 in contact with the second channel region.

Regarding claims 8-10, Figure 3 of Shimoji discloses a first control gate pattern (right side) and a second control gate pattern (left side) disposed over a semiconductor substrate 2, each of the first and second control gate patterns comprising a tunnel insulation pattern, a trap insulating pattern, a blocking insulation pattern and a control gate electrode 5 which are stacked sequentially; a first selection gate electrode 23 (right side) disposed, in parallel to the first control gate pattern, over the semiconductor substrate at one side of the first control gate pattern; a second selection gate electrode 23 (left side) disposed, in parallel to the second control gate pattern, over the substrate at one side of the second control gate pattern; a first gate insulation

pattern 8 interposed between the first selection gate electrode and the substrate, and between the first selection gate electrode and the first control gate pattern; a second gate insulation pattern 8 interposed between the second selection gate electrode and the semiconductor substrate, and between the second selection gate electrode and the second control gate pattern; a first cell channel region (right side) comprising a first channel region defined in the substrate under the first control gate pattern and a second channel region defined in the substrate under the first selection gate electrode; and a second cell channel region (left side) comprising a first cell channel region comprising a first channel region defined in the substrate under the second control gate pattern and a second channel region defined in the substrate under the second selection gate electrode, wherein the first and second selection gate electrodes are disposed symmetrically over the substrate. Note that region 6 under the control gates is an ONO layer (silicon oxide/silicon nitride/silicon oxide) (col. 5, lines 28-32). The first silicon oxide layer 6a is the tunnel insulating pattern, the silicon nitride layer 6b is the trap insulation pattern, and the second silicon oxide layer 6c is the blocking insulation pattern (for each control gate pattern).

Regarding claim 12, Figure 3 of Shimoji discloses the selection gate electrodes 23 are disposed between the control gate patterns.

Regarding claim 13, Figure 3 of Shimoji discloses a first drain 3 in contact with the first channel region of the first cell channel region (right side) and a source region 4 in contact with the second channel region of the first cell channel region (right side) and the second channel region of the second cell channel region (left side). Although not specifically shown in Figure 3, it is inherent that there is another drain region adjacent the second control gate pattern (left side).

Claims 1-3, 5, 8-10, 14, and 16 are rejected under 35 U.S.C. 102(e) as being anticipated by Kim et al. (US Pat. 6,784,476, hereinafter Kim).

Regarding claims 1-3, Figure 9J of Kim discloses a control gate pattern disposed over a semiconductor substrate 801 and comprising a tunnel insulation pattern, a trap insulation pattern, a blocking insulation pattern, and a control gate electrode 812', which are stacked; a selection gate electrode 806 disposed over the semiconductor substrate at one side of the control gate pattern; a gate insulation pattern 832 interposed between the selection gate electrode and the semiconductor substrate, and between the selection gate electrode and the control gate pattern; a cell channel region comprising a first channel region defined in the semiconductor substrate under the control gate pattern and a second channel region defined in the substrate under the selection gate electrode. Note that region 820 under the control gate is an ONO layer (silicon oxide/silicon nitride/silicon oxide) (col. 8, lines 11-14). The first silicon oxide layer is the tunnel insulating pattern, the silicon nitride layer is the trap insulation pattern, and the second silicon oxide layer is the blocking insulation pattern.

Regarding claim 5, Figure 9J of Kim discloses the thickness of the gate insulation pattern is less than the sum of the thickness of the tunnel insulation pattern, the trap insulation pattern, and the blocking insulation pattern.

Regarding claims 8-10, Figure 9J of Kim discloses a first control gate pattern (left side) and a second control gate pattern (right side) disposed over a semiconductor substrate 801, each of the first and second control gate patterns comprising a tunnel insulation pattern, a trap insulating pattern, a blocking insulation pattern and a control gate electrode 812' which are

stacked sequentially; a first selection gate electrode 806 (left side) disposed, in parallel to the first control gate pattern, over the semiconductor substrate at one side of the first control gate pattern; a second selection gate electrode 806 (right side) disposed, in parallel to the second control gate pattern, over the substrate at one side of the second control gate pattern; a first gate insulation pattern interposed between the first selection gate electrode and the substrate, and between the first selection gate electrode and the first control gate pattern; a second gate insulation pattern interposed between the second selection gate electrode and the semiconductor substrate, and between the second selection gate electrode and the second control gate pattern; a first cell channel region comprising a first channel region defined in the substrate under the first control gate pattern and a second channel region defined in the substrate under the first selection gate electrode; and a second cell channel region comprising a first cell channel region comprising a first channel region defined in the substrate under the second control gate pattern and a second channel region defined in the substrate under the second selection gate electrode, wherein the first and second selection gate electrodes are disposed symmetrically over the substrate. Note that region 820 under the control gates is an ONO layer (silicon oxide/silicon nitride/silicon oxide) (col. 8, lines 11-14). The first silicon oxide layer is the tunnel insulating pattern, the silicon nitride layer is the trap insulation pattern, and the second silicon oxide layer is the blocking insulation pattern (for each control gate pattern).

Regarding claim 14, Figure 9J of Kim discloses the control gate patterns are disposed between the selection gate electrodes 806.

Regarding claim 16, Figure 9J of Kim discloses the thickness of each gate insulation pattern is less than the total thickness of the tunnel insulation pattern, the trap insulation pattern, and the blocking insulation pattern.

Claims 1-6, 8-10, 11, and 14-16 are rejected under 35 U.S.C. 102(e) as being anticipated by Kawahara et al. (US Pat. 6,785,165, hereinafter Kawa).

Regarding claims 1, Figures 4 and 6 of Kawa disclose a control gate pattern disposed over a semiconductor substrate and comprising a tunnel insulation pattern BOTOX, a trap insulation pattern SIN, a blocking insulation pattern TOPOX, and a control gate electrode MG, which are stacked; a selection gate electrode SG disposed over the semiconductor substrate at one side of the control gate pattern; a gate insulation pattern STOX/GAPOX interposed between the selection gate electrode and the semiconductor substrate, and between the selection gate electrode and the control gate pattern; a cell channel region comprising a first channel region defined in the semiconductor substrate under the control gate pattern and a second channel region defined in the substrate under the selection gate electrode.

Regarding claims 2 and 3, Kawa discloses the tunnel insulation pattern BOTOX is formed of silicon oxide and the trap insulation pattern SIN is formed of silicon nitride (col. 10, lines 35-42).

Regarding claim 4, Figure 4 of Kawa discloses the selection gate electrode SG is spacer-shaped and elongated to cover one sidewall and a top surface of the control gate pattern. Note that the selection gate electrode SG of Kawa can be considered to be spacer-shaped since a spacer can have virtually any shape.

Regarding claim 5, Figure 4 of Kawa discloses the thickness of the gate insulation pattern STOX/GAPOX is less than the sum of the thickness of the tunnel insulation pattern BOTOX, the trap insulation pattern SIN and the blocking insulation pattern TOPOX.

Regarding claim 6, Figure 4 of Kawa discloses a drain region MD in contact with the first channel region and a source region MS in contact with the second channel region.

Regarding claim 8, Figures 38-45 of Kawa disclose a first control gate pattern (left side) and a second control gate pattern (right side) disposed over a semiconductor substrate, each of the first and second control gate patterns comprising a tunnel insulation pattern BOTOX, a trap insulating pattern SIN, a blocking insulation pattern TOPOX, and a control gate electrode (MG1 and MG2) which are stacked sequentially; a first selection gate electrode SG1 disposed, in parallel to the first control gate pattern, over the semiconductor substrate at one side of the first control gate pattern; a second selection gate electrode SG2 disposed, in parallel to the second control gate pattern, over the substrate at one side of the second control gate pattern; a first gate insulation pattern STOX/GAPSW/CAP interposed between the first selection gate electrode and the substrate, and between the first selection gate electrode and the first control gate pattern; a second gate insulation pattern STOX/GAPSW/CAP interposed between the second selection gate electrode and the semiconductor substrate, and between the second selection gate electrode and the second control gate pattern; a first cell channel region comprising a first channel region defined in the substrate under the first control gate pattern and a second channel region defined in the substrate under the first selection gate electrode; and a second cell channel region comprising a first cell channel region comprising a first channel region defined in the substrate under the second control gate pattern and a second channel region defined in the substrate under

the second selection gate electrode, wherein the first and second selection gate electrodes are disposed symmetrically over the substrate.

Regarding claims 9 and 10, Kawa discloses the tunnel insulation pattern BOTOX is formed of silicon oxide and the trap insulation pattern SIN is formed of silicon nitride (col. 10, lines 35-42).

Regarding claim 11, Figure 45 of Kawa discloses the first and second selection gate electrodes (SG1 and SG2) are spacer-shaped and elongated to cover one sidewall and a top surface of the control gate patterns. Note that the selection gate electrodes of Kawa can be considered to be spacer-shaped since a spacer can have virtually any shape.

Regarding claim 14, Figures 38-45 of Kawa disclose the control gate patterns are disposed between the selection gate electrodes.

Regarding claim 15, Figures 38-45 of Kawa disclose a first source region MSM (left side) in contact with the second channel region of the first cell channel region; a second source region MSM (right side) in contact with second channel region of the second cell channel region; a drain region MDM in contact with the first channel region of the first cell channel region and the first channel region of the second cell channel region.

Regarding claim 16, Figure 4 of Kawa discloses the thickness of the gate insulation pattern STOX/GAPOX is less than the sum of the thickness of the tunnel insulation pattern BOTOX, the trap insulation pattern SIN and the blocking insulation pattern TOPOX.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kawa.

Regarding claim 7, Figure 45 of Kawa discloses a metal silicide (cobalt silicide) formed over a predetermined region of a sidewall of the selection gate electrode SG1 and a surface of the drain/source regions (col. 25, lines 28-33). Kawa does not explicitly disclose a metal silicide on a sidewall of the control gate. However, as shown in Figure 6, a wiring M1b is connected to an upper surface of the control gate MG. Since control gate is made of polysilicon (col. 10, lines 42-44), it would have been obvious to the ordinary artisan at the time the invention was made to use a metal silicide between the wiring and the gate for the purpose of lowering the contact resistance, which is well known in the art. Note the top surface of the gate can be considered a sidewall because the top surface is a side (i.e., top side).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew C. Landau whose telephone number is (571) 272-1731.

The examiner can normally be reached from 8:30 AM - 5:30 PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached

on (571) 272-1664. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9306 for regular communications and (703) 872-9306 for After Final communications.

Matthew C. Landau

Examiner

April 22, 2005

TOM THOMAS
SUPERVISORY PATENT EXAMINER